HIGH-PERFORMANCE-SENSORSYSTEME durch Verbindung von Siliziumtechnologie und keramischer Mehrlagentechnik

HIPS | HIGH PERFORMANCE SENSORS

Powered by SiCer - The best of both worlds

Silicon-ceramic composite substrates - from the laboratory to a robust process technology

Marc Bochard | VIA electronic GmbH

Cathleen Kleinholz | Technische Universität Ilmenau

Agenda

1. Introduction
2. Manufacturing process of SiCer-substrats
3. Fabrication of cavities
   1. in ceramic
   2. in silicon
4. Layout and process optimization
5. Analysis and measurement results
6. Conclusion and Outlook

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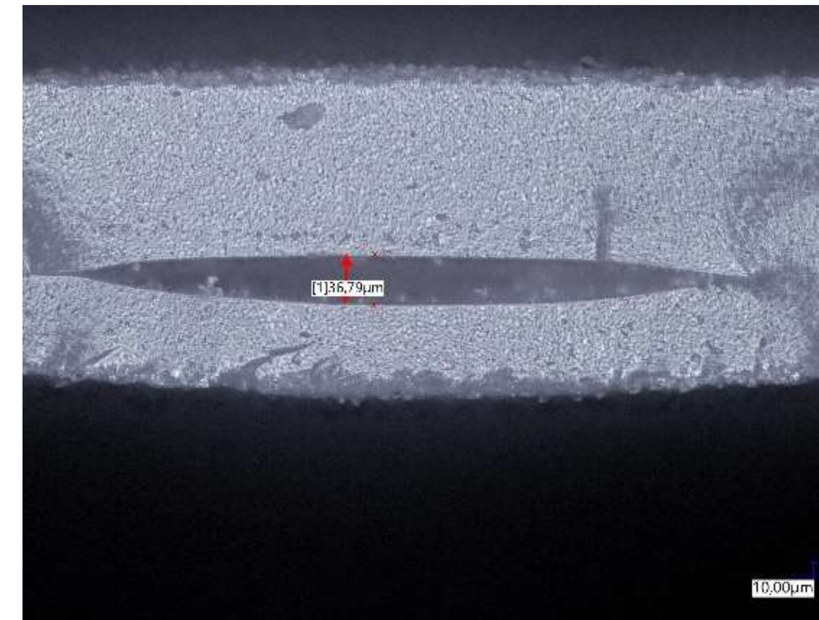
Advantages and special properties of SiCer sensor applications:

- high temperature stability
- manufacturing and 3D-integration at wafer-level
- high bond strength at the interface



Ceramic membrane after sintering process

Challenges:

- manufacturing and stability of cavities geometry
- (in one or both materials)
- defect-free bonding-interface

→ **process optimization necessary**

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- State of the art in SiCer technology and beyond

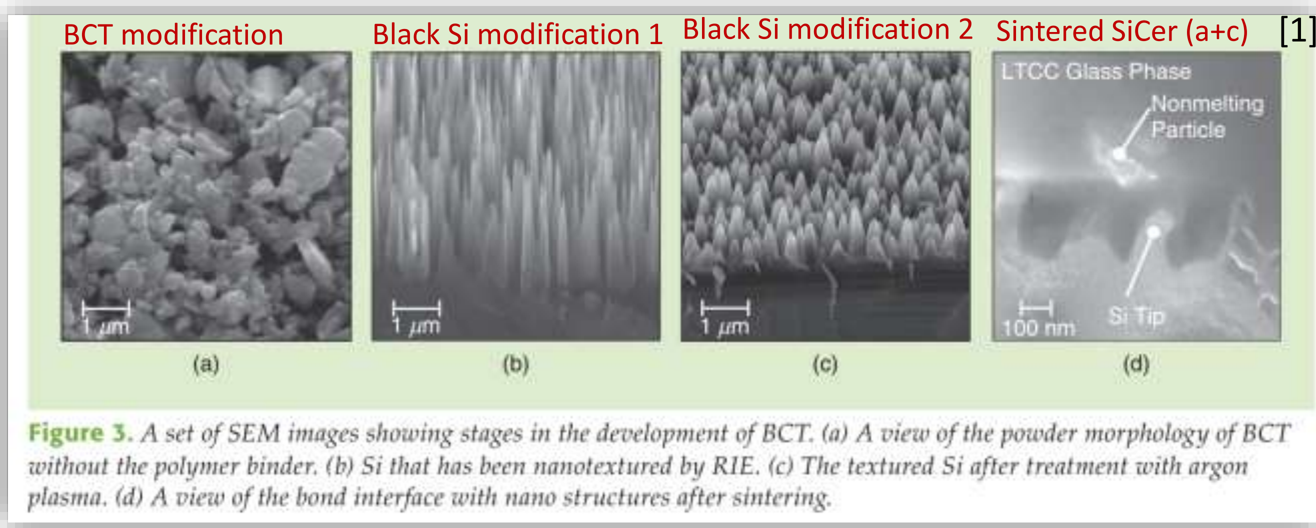
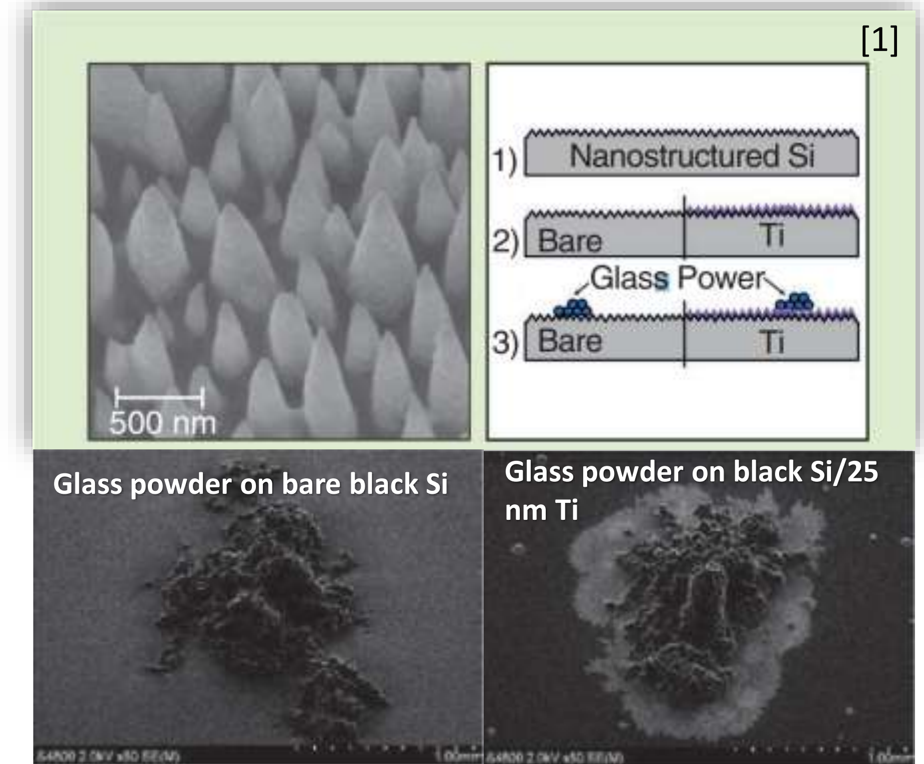


Figure 3. A set of SEM images showing stages in the development of BCT. (a) A view of the powder morphology of BCT without the polymer binder. (b) Si that has been nanotextured by RIE. (c) The textured Si after treatment with argon plasma. (d) A view of the bond interface with nano structures after sintering.

BCT6
quartz as non melting filler / sodium-free glass component
DINCH plasticizer (1.2-cyclohexane dicarboxylic acid diisononyl ester)



To improve the bonding between Si and Cer, the wetting must be increased.

TiO2 as adhesion promoter (increasing hydrophilicity)

TiO2 layer + nanostructuring enhance the bonding significantly by increasing the wettability

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2. SiCer Manufacturing process

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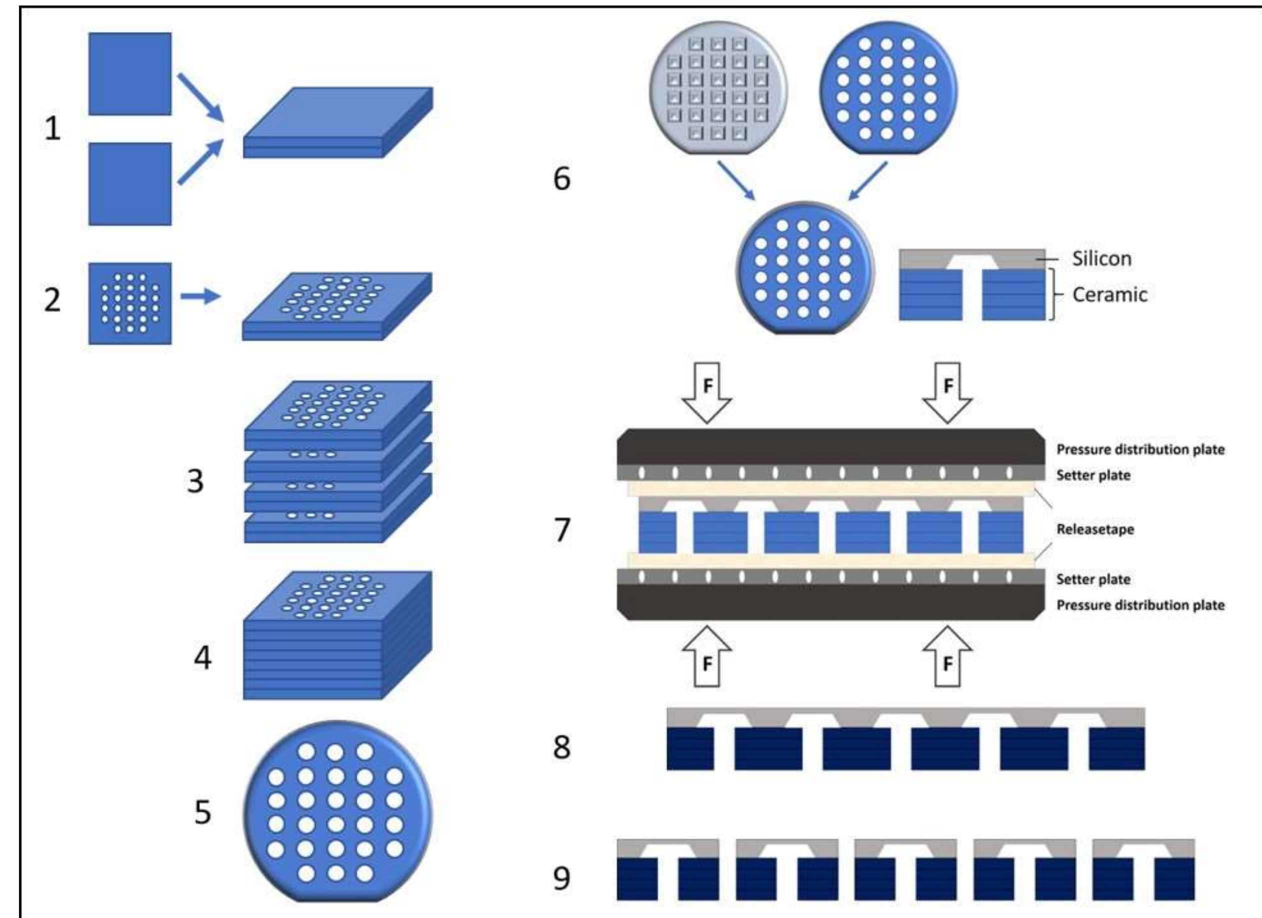
1. tape preparation
2. punching of cavities, screen printing, via filling
3. stacking of double tapes (for process stability)
4. isostatic lamination
5. laser cutting or punching of wafer contour
6. SiCer stacking
7. sinter process
8. post-processing
9. single chip module



Process sequence of SiCer-substrate production [3]

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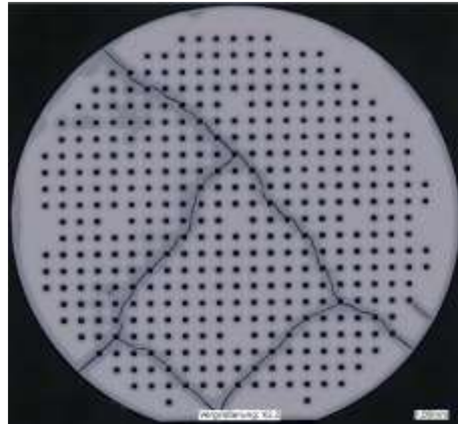
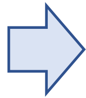
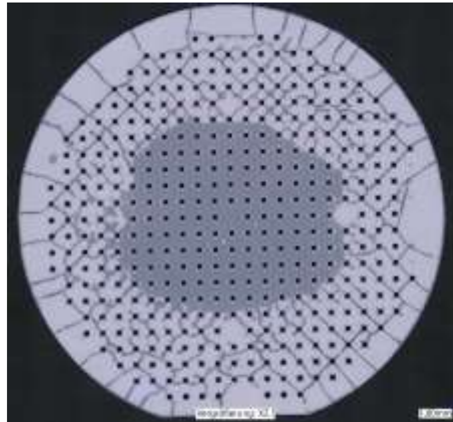
- Towards defect-free SiCer composite with open cavities

Light grey: Insuffisant or inexistant bonding
Dark grey: Good bonding

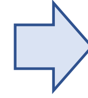


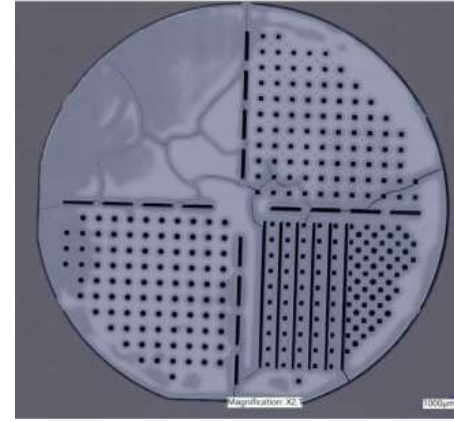
Cracking, insufficient bonding



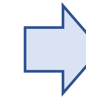


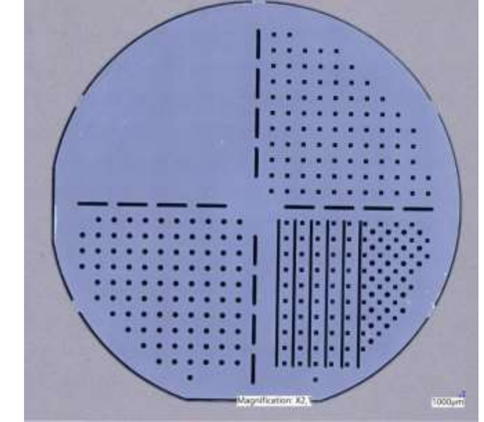
In parts better adhesion, more cracking on the outer side





In parts better adhesion, Significantly less cracking





No cracks, defect-free bond

Lamination process adaptation:
Higher pressure
Higher temperature
Longer process duration

Cavity structure modification to relax the mechanical stress during sintering

Cavity structure modification to relax the mechanical stress during sintering – 1 single sheet

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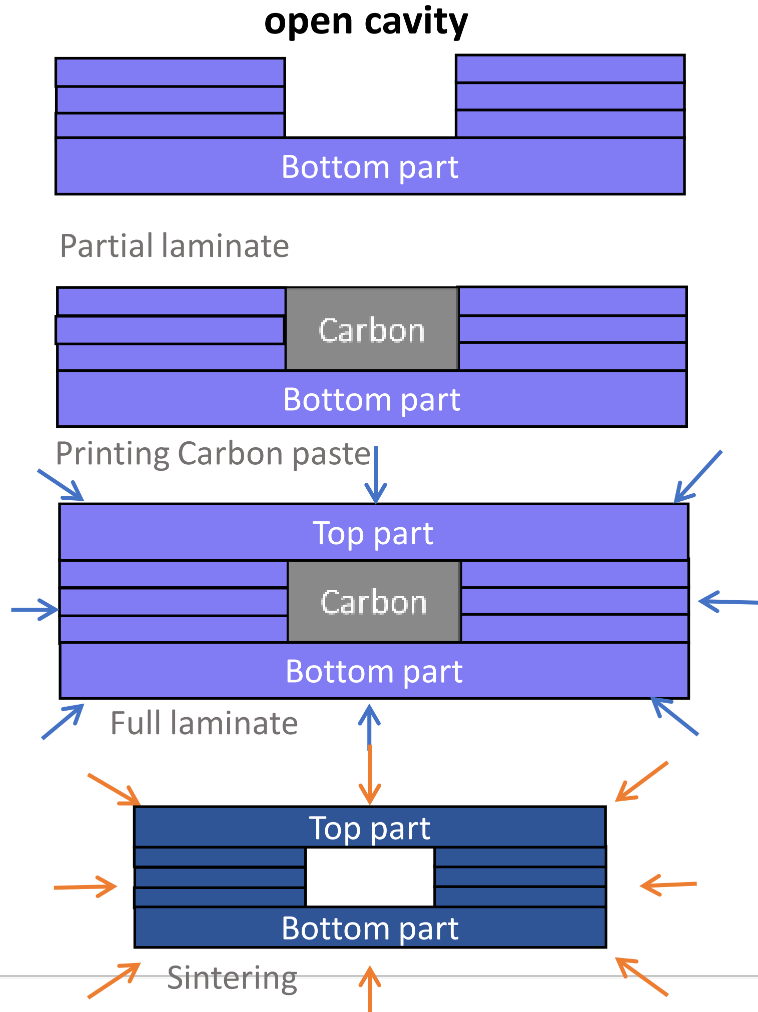
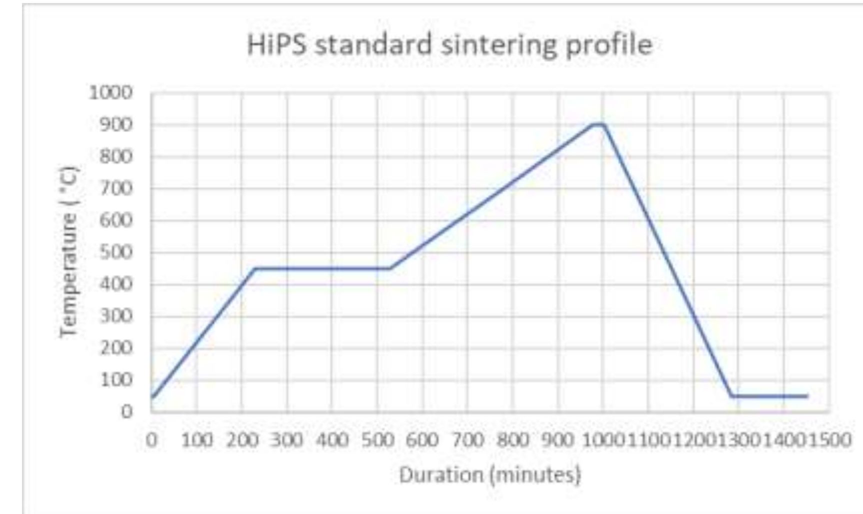
3. Fabrication of cavities – ceramic side

Process flow for the isostatic lamination method with sacrificial carbon paste





A failed attempt by EPFL, Switzerland [2]

Sintering profile needs to be modifed to enable carbon burn out before the pore closure.

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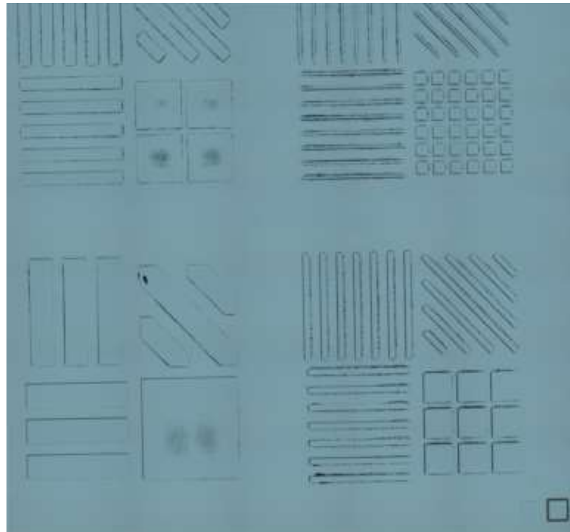
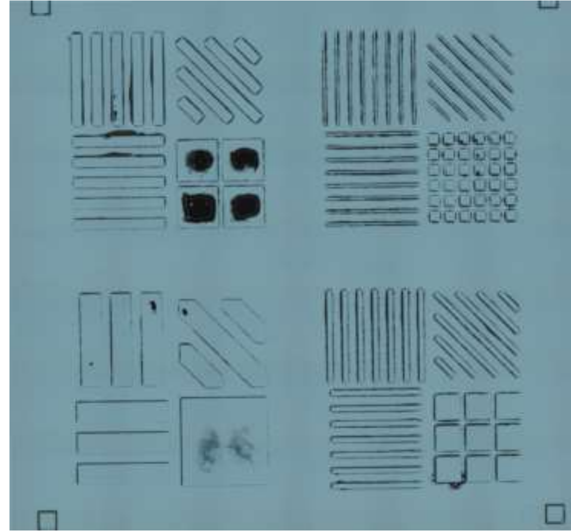
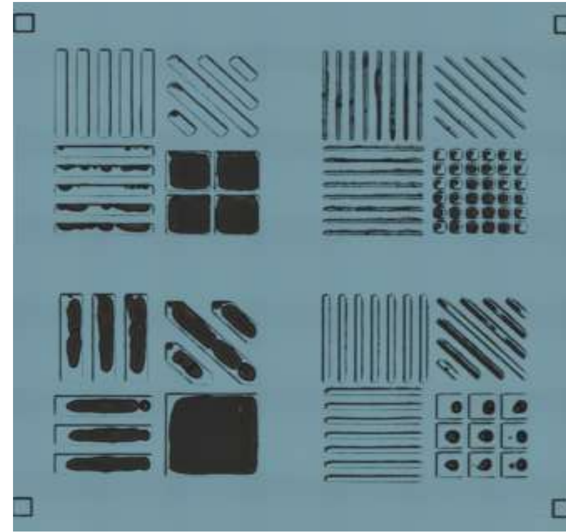
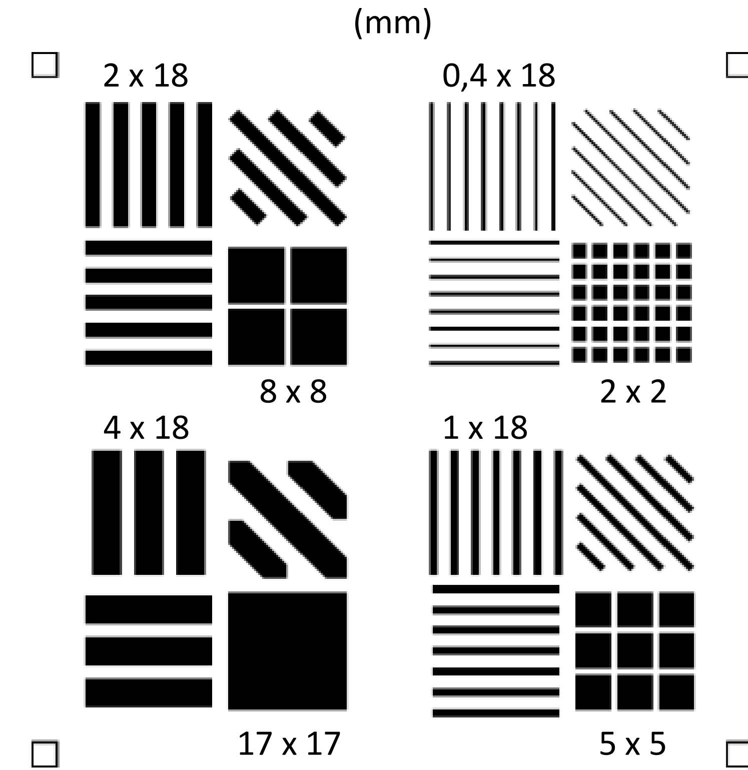
3. Fabrication of cavities – ceramic side

Filling deep cavities by **screen printing** of carbon paste_ green state


First print


Second print


Third print



Solutions:

- use stencil instead of screen
- Depending on the depth of the cavities, the printing process must be must be adjusted

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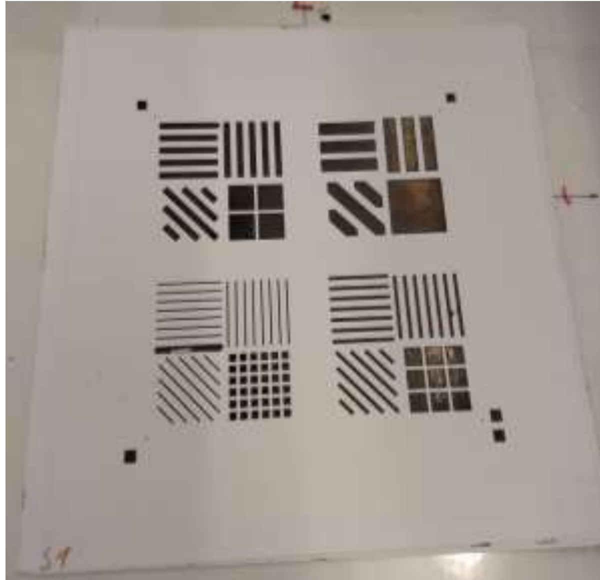
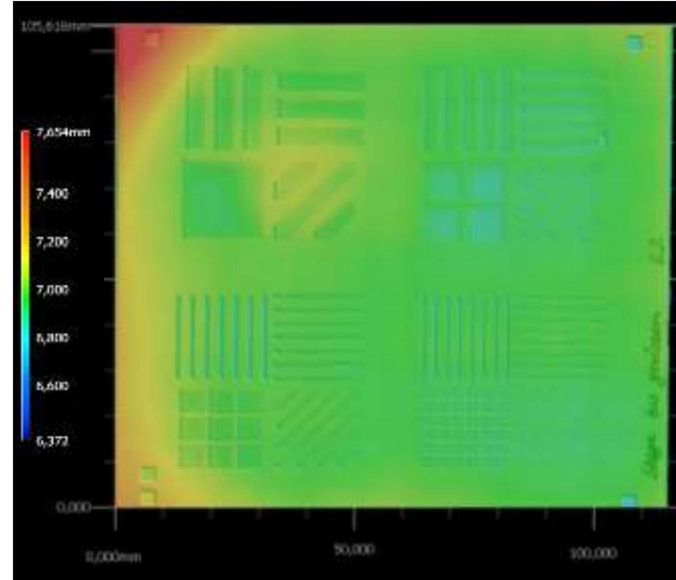
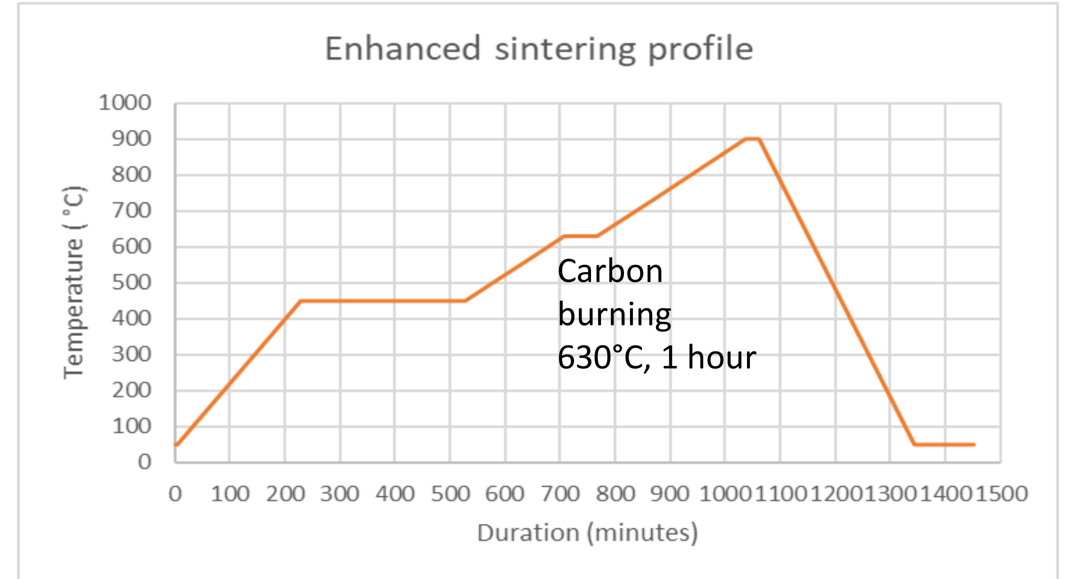
3. Fabrication of cavities – ceramic side

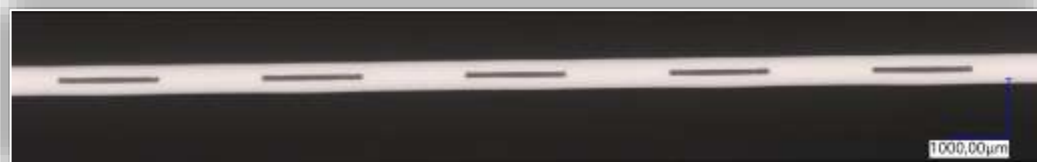


Filling the cavities
Stencil printing



Full laminate





Sintered (1h burning out phase at 630°C added)

Layer	Material	Thickness green [µm]	Size
1-5	BCT6	ca. 250	115x115

Each layer is created with 2 BCT6 tapes

Shrinkage ratio in Z direction: ~50%

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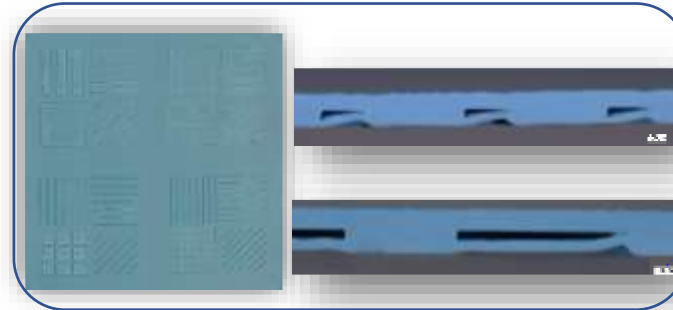
Structural elements:

- Buried channels and cavities
- DP951 PX and BCT6

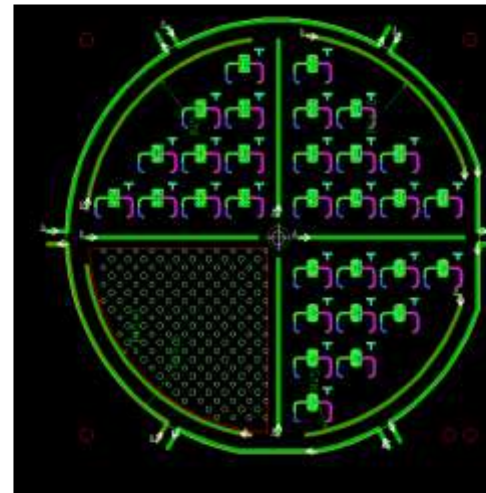
Cavities deformed => not well filled

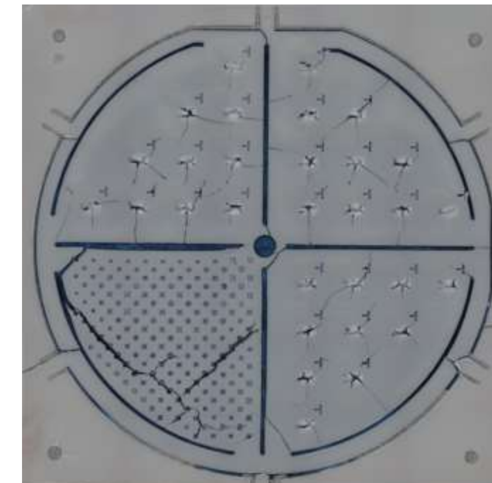


DP951, Screen printed carbon paste

BCT6, Stencil printed carbon paste

- 6 LTCC layers (each layer created with 2 BCT6 tapes) bonded to Si
- Reaction and mixing chamber for microfluidics
- Crack formation at wafer level
- Relatively good bonding between LTCC and Si





SiCer test structure with integrated fluidics

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3. Fabrication of cavities – silicon side

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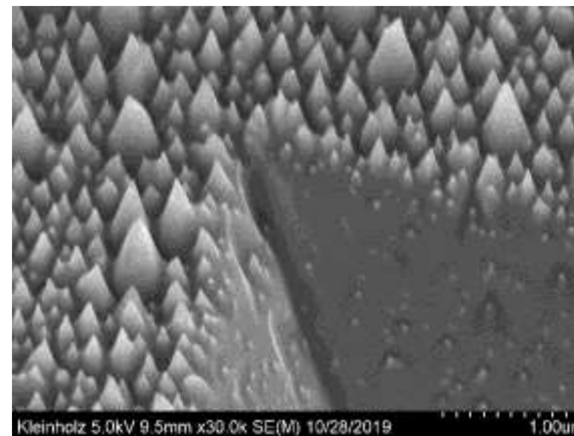
Silicon pre-processing:

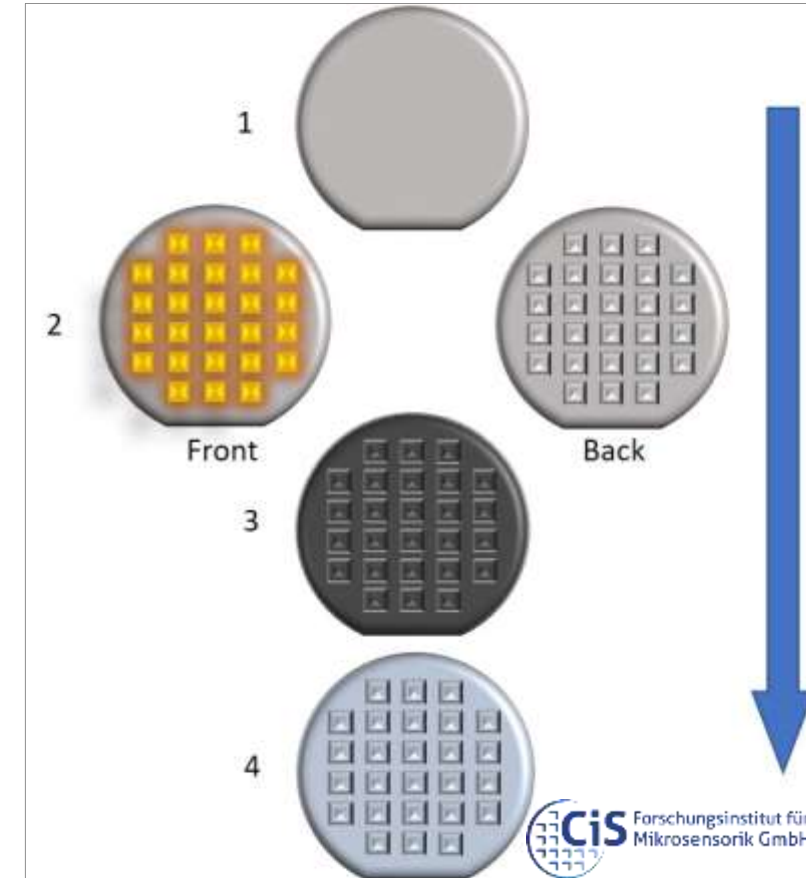
1. 4 inch silicon wafer, unprocessed
2. Front: processing of contact pads, piezoresistive resistors, etc.
   Back: etching of membrane using KOH
3. applying black silicon at backside (optional)
4. sputtering of Ti layer at backside and oxidation to TiO_2

Black Silicon:

- optimized RIE process
- criteria:
  - no mountain formations
  - homogeneity across the wafer
  - specific needle height and width matched to the ceramic tape



Si surface after RIE processing



Silicon preprocessing [3]

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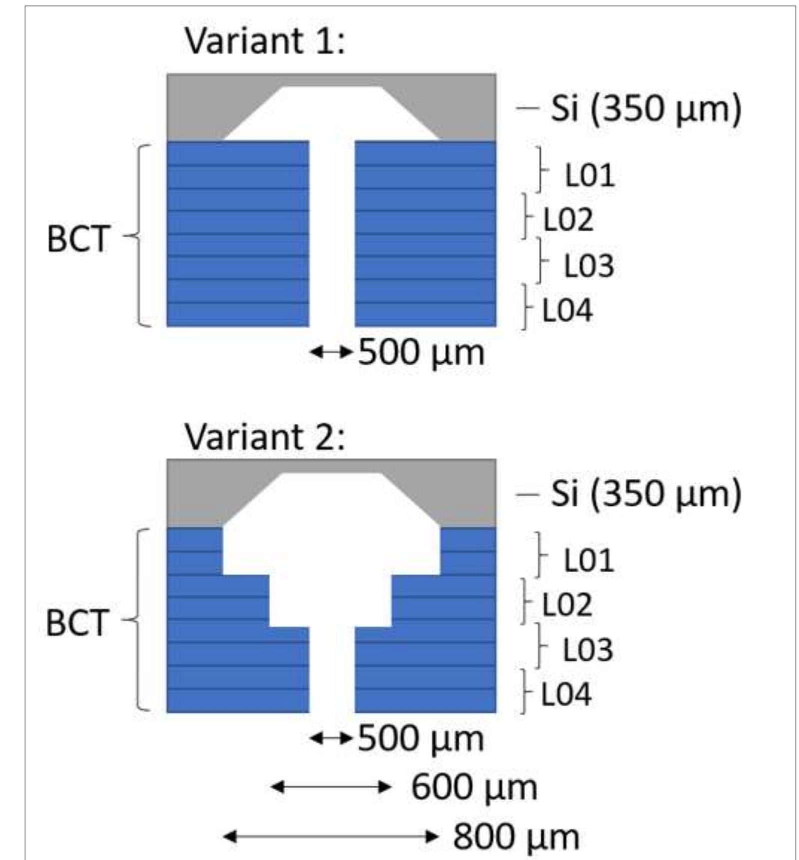
4. Layout and process optimization

- additional way to stabilise cavities by implementing sequential lamination
  - standard: punched double tapes are stacked and laminated
  - sequential: double tapes are individually laminated together

- production of two test layouts
  - V1: 500 µm straight channel towards Si
  - V2: widening channel, starting with 500 µm up to 800 µm

- seq. Lamination:
  - (1) L03+L04 → L034
  - (2) L02+L034 → L0234
  - (3) W+L01 → WL01
  - (4) WL01+L0234+Releasetape → WL01234R



Different ceramic channel construction [3]

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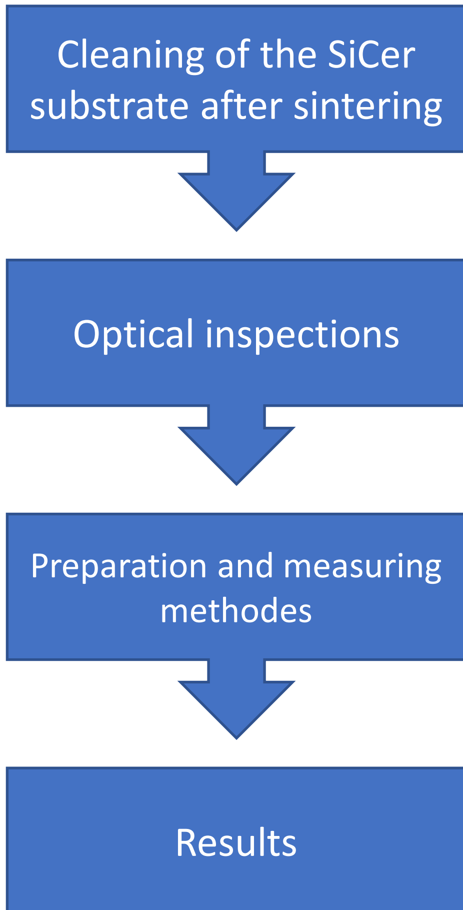
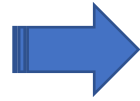
5. Analysis and measurement results





<u>two-step cleaning process:</u>

- preliminary cleaning
- fine cleaning

Preliminary:

- Water rinsing to remove loose releasetape particles

Fine cleaning:

- solvent cleaning in ultrasonic bath
- bake out

SiCer substrate with loose releasetape on both sides

Final SiCer substrate after cleaning process

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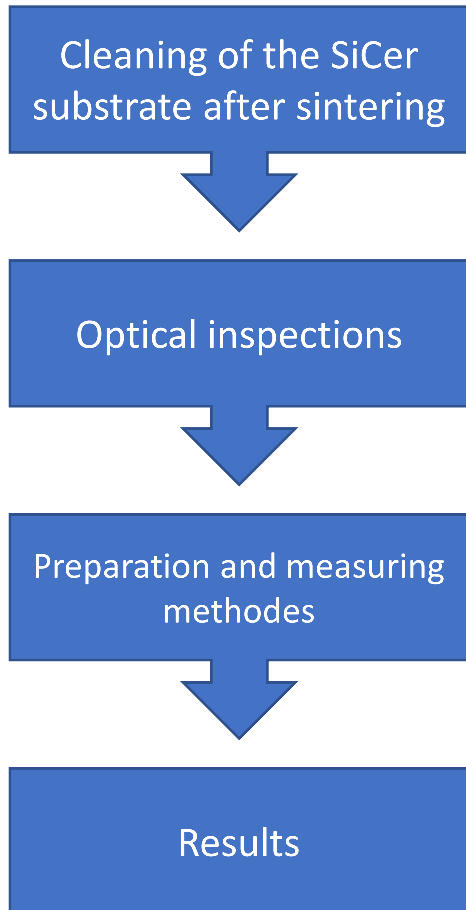
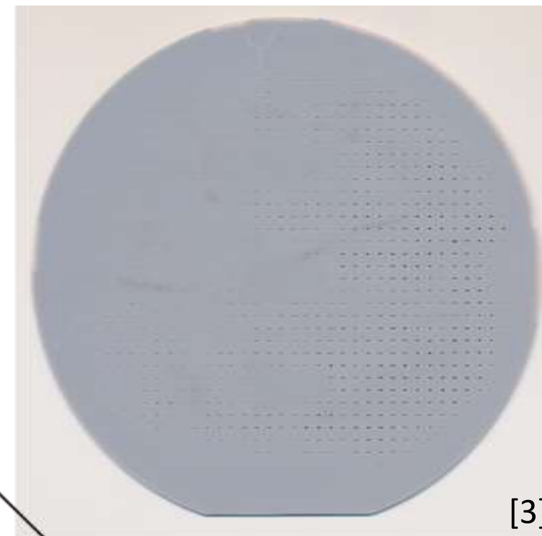
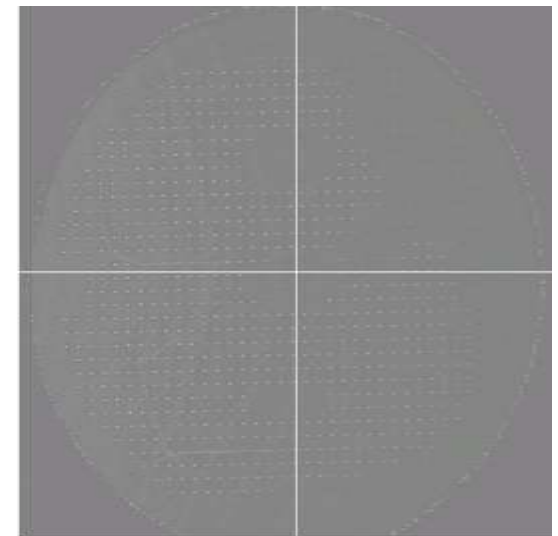
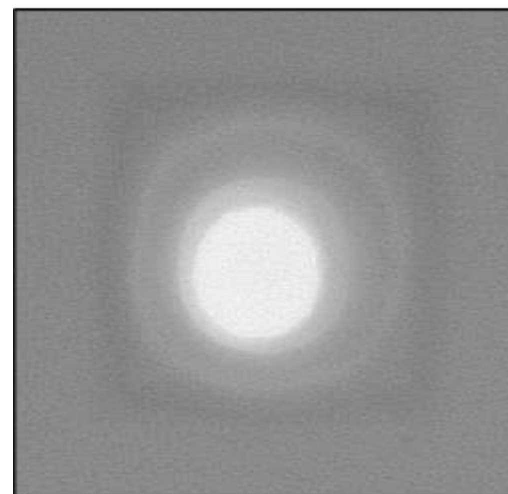


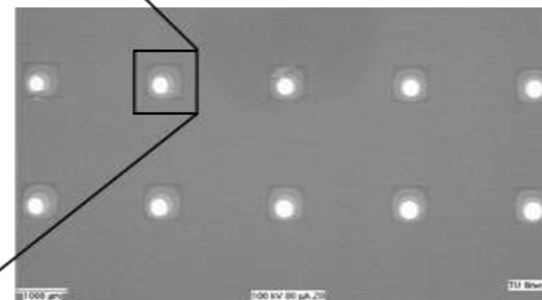
Wafer-level inspection:

- imaging
- ultrasonic micrsoscopy
- x-ray examination
- bow measurement









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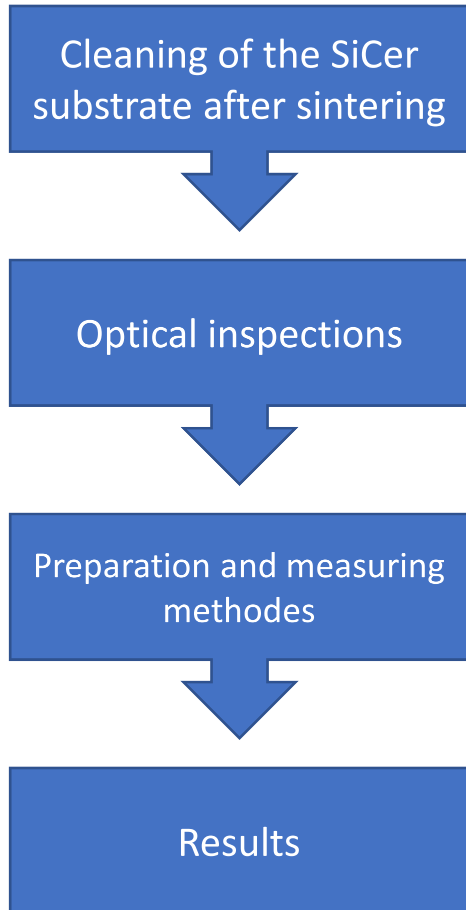


<u>Chip-level examination:</u>

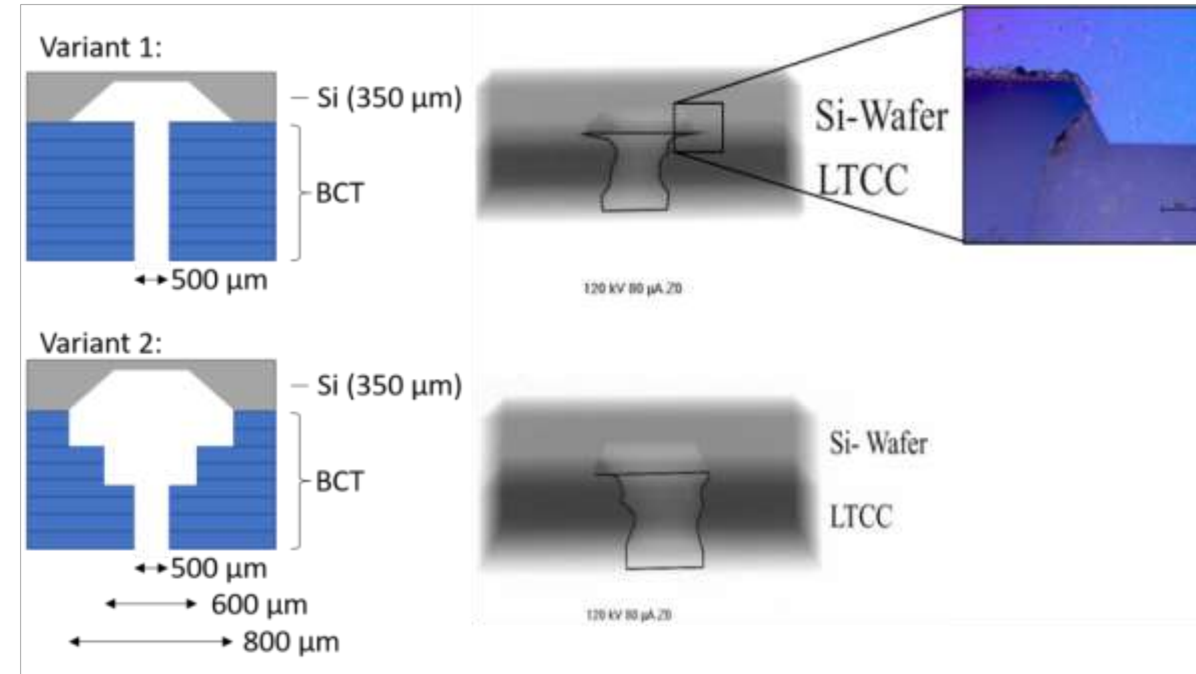
- cross-sectional view
- burst pressure method

cross-sectional view:

- Microscopy
- EDX

burst pressure method:

- destructive test method
- chip is glued onto special holder and tested up to max. pressure or bursting of sample
- measuring range limited to 400 bar



Cross-sectional view of both ceramic channel layouts after sintering process [3]

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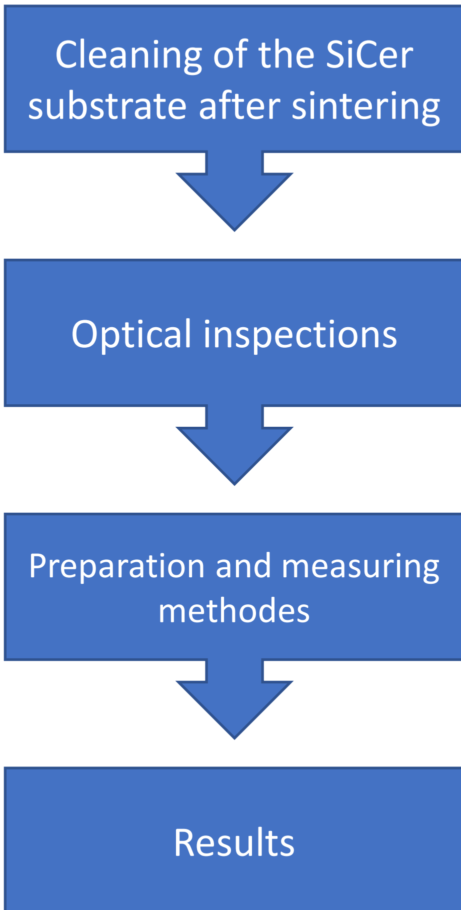
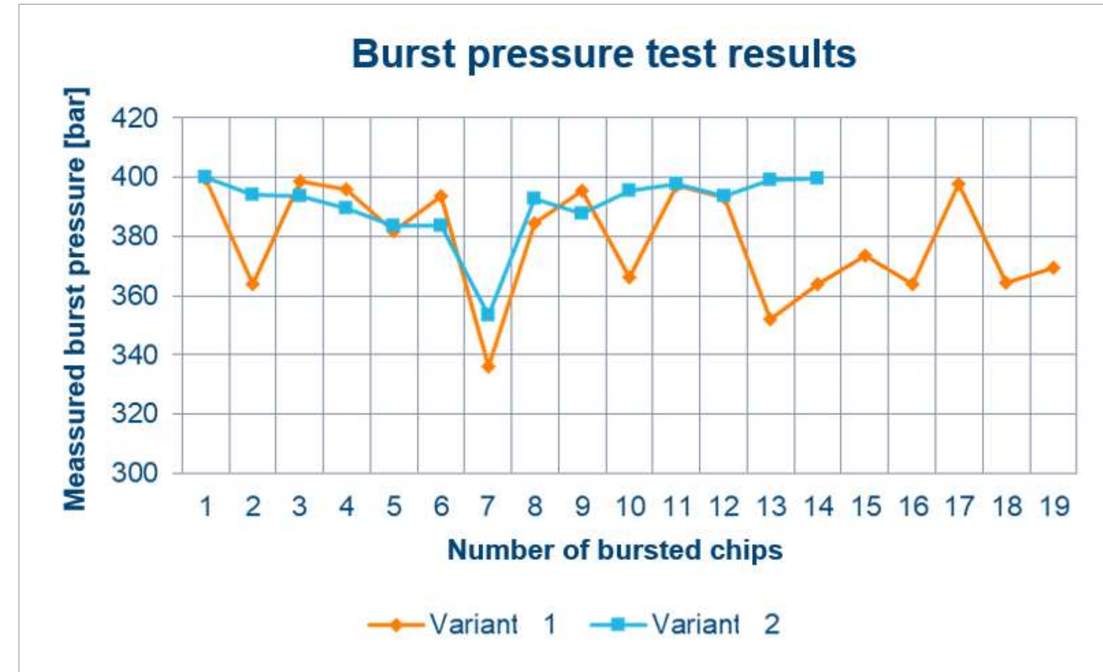


- total amount of 30 samples each tested
- typical fracture pattern or failures:
  - fracture at bondinterface
  - bulk material fracture
  - detaching of adhesive bond

two exemplary fracture pattern (left: fracture at bondinterface,
right: bulk material fracture) [3]



Comparison of both ceramic layout variants [3]

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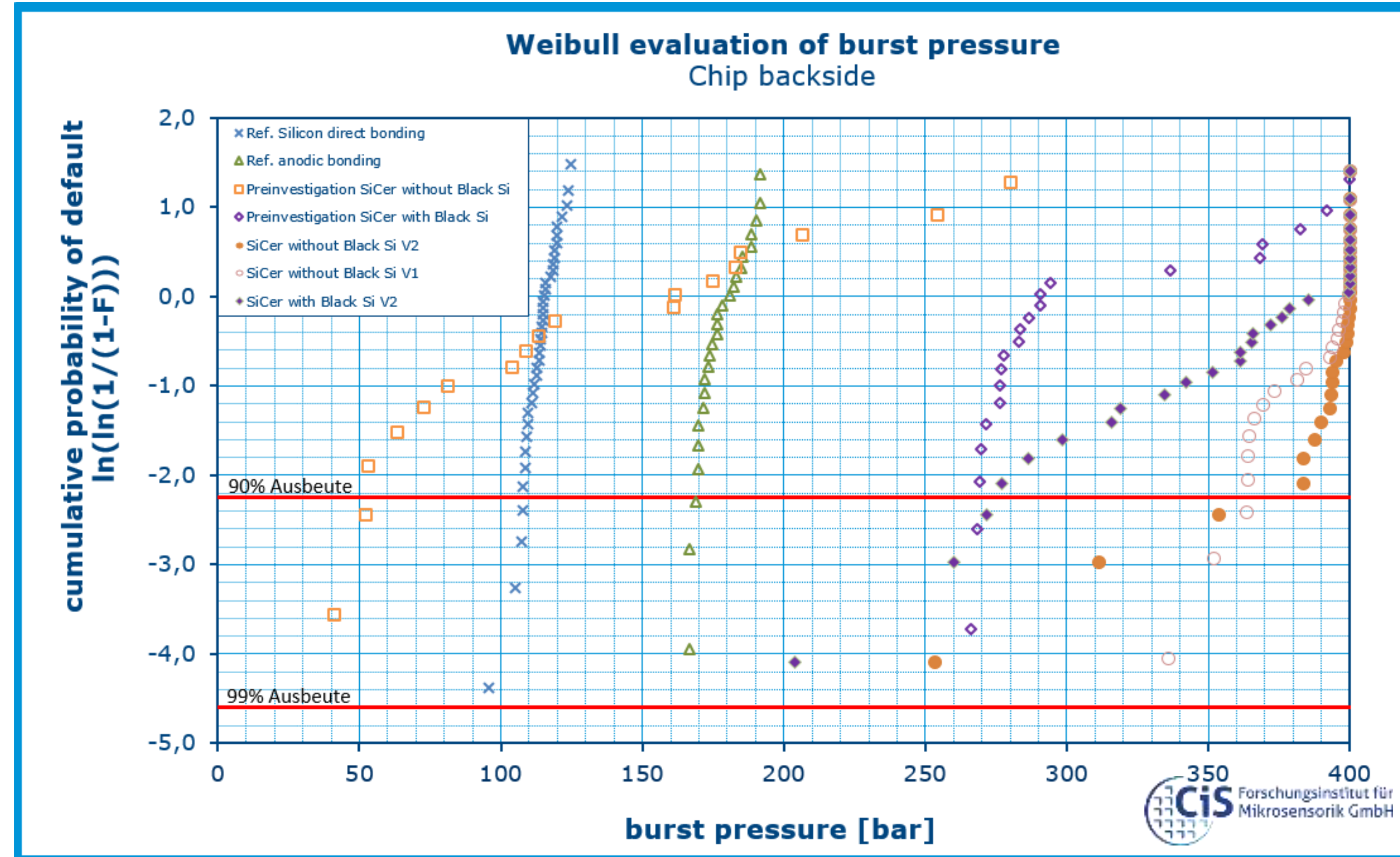
6. Conclusion and Outlook

- in total 7 measurement series, 5 with SiCer substrates
- clear improvement of burst pressure results with SiCer
- Best results achieved with ● measurement series

→ widening channel and without black silicon at bondinterface



Burst pressure measuring results from different test samples [4]

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6. Conclusion and Outlook

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- Fluidic structures can be created at LTCC level with excellent shape by using carbon paste
- Bonding process has been evaluated and adapted to successfully bond Si and structured Ceramic wafers
- SiCer-substrates show increase of bonding strength at interface
- enlarging ceramic channel resolts in lower burst failure
- Black Silicon not necessarily needed for pressure sensors manufactured by pressure sintering process

References:

- [1] M. Fischer, et al.– Silicon-Ceramic Composite Substrate: A Promising RF Platform for Heterogeneous Integrations, IEEE Microwave Magazine 20, (DOI: 10.1109/MMM.2019.2928675), 28-34, 2019
- [2] Y. Fournier, – 3D Structuration Techniques of LTCC for Microsystems Applications, PhD Dissertation, Swiss Federal Institute of Technology Lausanne (EPFL), 2010
- [3] C. Kleinholz, et al.: Implementation of SiCer technology for pressure sensor applications, CICMT Conference; 26.-29.04.2021
- [4] A. Cyriax, C. Kleinholz: Anwendungen von SiCer-Substraten bei Drucksensoren, HIPS Statusworkshop; 07.04.2021

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VIA electronic GmbH

+ 49 36601 9298 114

m.bochard@via-electronic.de

www.via-electronic.de

Technische Universität Ilmenau

+ 49 3677 693385

cathleen.kleinholz@tu-ilmenau.de

www.tu-ilmenau.de/mne-et/

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